DETERMINISTIC HARDWARE RESET FOR FRC MACHINE

Abstract of the Disclosure

A processor includes one or more execution cores, each execution core having an associated scan chain to provide data to a set of voltage nodes of the core. A reset module drives a data pattern onto the scan line, responsive to a reset event. The data pattern places the set of voltage nodes of each execution core into specified logic states. For a processor including multiple execution cores configured to operate in an FRC mode, identical data patterns are driven onto the scan chains to reduce indeterminacy in the reset machine state of the processor.